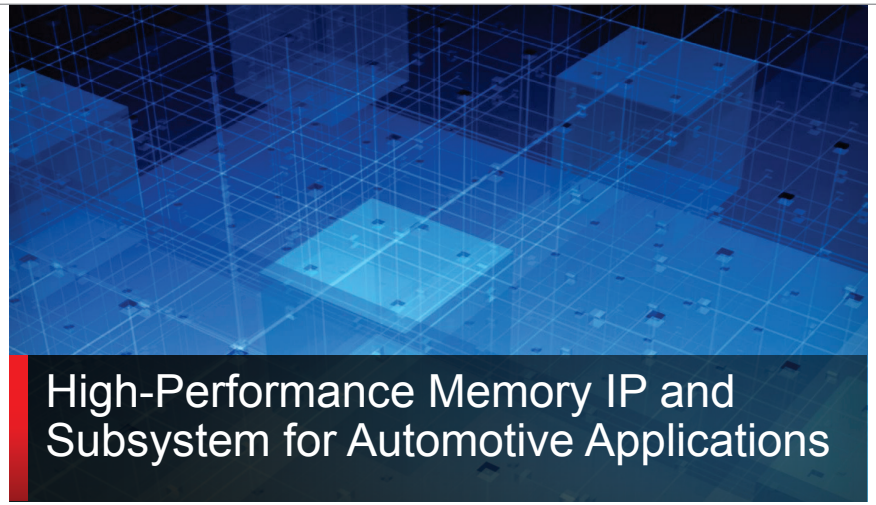
High-Performance Memory IP and Subsystem for Automotive Applications

Cadence Design Systems

ABSTRACT

Demand for Automotive electronics has accelerated starting with the need of feature rich infotainment system to mainstream adoption of ADAS to fully autonomous driving. Today's on vehicle applications require high performance, high bandwidth computing. Especially due to the high data rate in camera-based and other sensor fusion systems, the DDR interface in ADAS SoCs is critical and require utmost performance to process uncompressed video and sensor data. DDR memory is a key IP to enable these capabilities in modern automobiles. The presentation will discuss why LPDDR4 SDRAM has become the choice of memory over the DDR4 or DDR3, how ECC coverage is maintained across this transition, together with considerations for a memory sub-system that is high performance, robust, and functional safety compliant. Additionally, we will share with you design measures that are needed to meet automotive temperature requirements, additional reliability requirements and conformance to ISO26262 requirements as well as AEC-Q100 specifications and silicon data for such implementation in 16nm and 7nm.



High-Performance Memory IP and Subsystem for Automotive Applications

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TSMC OIP 2017
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Agenda

1. Automotive Applications Driving Memory Bandwidth
2. Choice of DRAM and Memory Subsystems
3. DDR Interface IP – Certifications and Design to Grade
4. Active Safety Enhancements in IP
5. Conclusion

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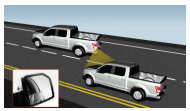
Automotive Safety Evolution
Main Goal - Avoid Crash, Injury, Fatality

Advanced driver assists from being offered in high-end luxury vehicles to being offered in the majority of new cars in just one model year

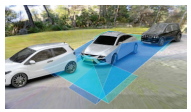
Collision Warning/Avoidance

Pedestrian Detection Warning



Blind Spot Monitor

Night Vision



Surround View Camera

Parking Asist

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New Applications Drive Complex Electronics

- Balanced growth in overall automotive semiconductor
- Significant growth for ADAS and infotainment applications

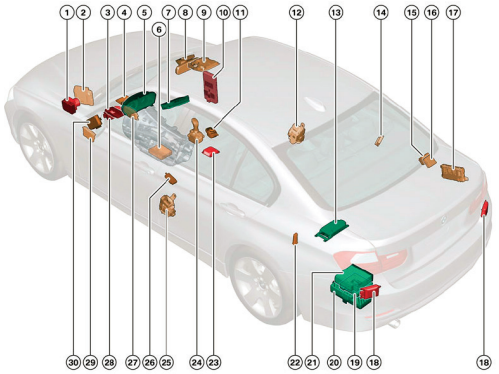

Image courtesy of BIMMERPOST.com F30 General Vehicle Electronics

Index	Explanation
1	Dynamic Stability Control (DSC)
2	Digital Motor Electronics (DME)
3	Vertical Dynamics Management (VDM)
4	Integrated automatic heating / air conditioning (IHKA)
5	Instrument panel (KOMBI)
6	Electronic transmission control (EGS)
7	Head unit
8	High-beam assistant (FLA)
9	Roof function center (FZD)
10	Front Electronic Module (FEM)
11	Controller (CON)
12	Reversible electric automatic reel right (REMA RE) (not for US)
13	Combox
14	Electronic fuel pump control (EKPS)
15	Parking Maneuvering Assistant (PMA)
16	DC/DC converter
17	Rear Electronic Module (REM)
18	Blind spot detection (SWW)
19	Video module VM (not for US)
20	Hi-Fi amplifier AMP/Top-HiFi amplifier (AMPT)
21	DVD changer (DVDC)
22	Tire Pressure Monitoring System (TPMS)
23	Integrated Chassis Management (ICM)
24	Gear selector switch (GWS)
25	Reversible electric automatic reel left (REMA LI) (not for US)
26	Driver's seat module (SMFA)
27	Advanced Crash Safety Module (ACSM)
28	Electronic Power Steering (electromechanical power steering) (EPS)
29	Camera-based driver support systems (KAFAS)
30	Control unit for camera systems (TRSVC)

More and more electronics added for infotainment and ADAS

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Diversity and Complexity of ADAS Applications

Drives need for a high-performance DRAM-based memory

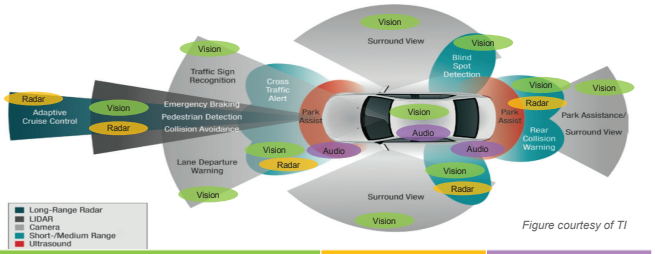

Figure courtesy of TI

Vision		Radar	Audio/Sound
Rear-View Camera Vision Enhancement Auto-Dimming Headlights Blind-Spot Detection 360 View Parking Assist Sign Recognition Traffic Signal Detection	Lane Detection Rain/Fog Detection Pedestrian Detection Pedestrian Avoidance Eye Focus Detection Driver Monitoring Sign Recognition Vehicle Detection	Front Collision Avoidance Braking Adaptive Cruise Control 360-Degree Hazard Awareness Rear Collision Detection	Rear Object Detection Parking Assist/Auto Park Voice Recognition Cabin Noise Reduction Emergency Recognition

- Complex processing and data manipulation needs large and fast memories, SRAM is not sufficient… enter DRAM

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Issues with Adopting DRAM for Automotive

Memory and DDR IP vendors stepping up

- Traditional DRAM temp range is limited
  - Extended temp range for LPDDR4 is now available from major vendors
- DRAM is fundamentally a capacitor holding charge
  - Long considered not reliable enough for automotive
  - System ECC and command/address parity protection are important
  - Code stored in DRAM needs additional protection
- DDR controller support for ECC and data/address parity critical
- IP compliance to automotive grade and safety certification are requirements

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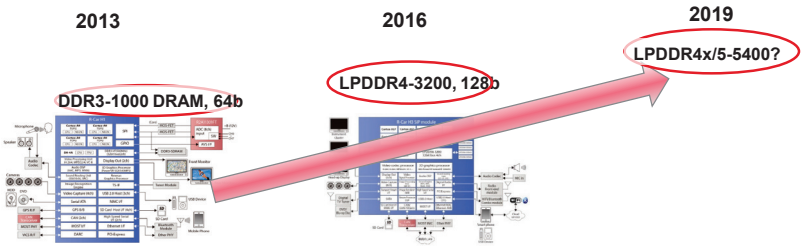
Memory Bandwidth and Capacity Needs for ADAS

High bandwidth and modest capacity



https://www.renesas.com/en-us/solutions/automotive/products/rcar-h1.html
https://www.renesas.com/en-us/solutions/automotive/products/rcar-h3.html

- Vision processing is bandwidth hungry
  - Frame rates, resolution and #streams rising
  - Example: 8MP camera, 60 fps, 16 bit depth => 1GBps
- Storage requirement for ADAS is moderate compared to server/ mobile
  - Smaller footprint RTOS
- Silicon proven DDR IP at highest data rates is critical

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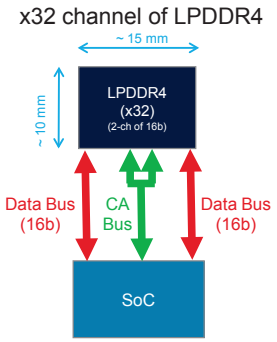
LPDDR4 Automotive System Example

- X32 channel
- Total band width: 17 GBps
- Memory capacity : 4Gb-16Gb
- Total DRAM Area: ~ 150 mm2

- Advantages:
  - Highest bandwidth and data rate
  - X32 devices
  - Better bandwidth/capacity ratio suited for ADAS
  - Compact DRAM Area: ~ 150 mm²/ch

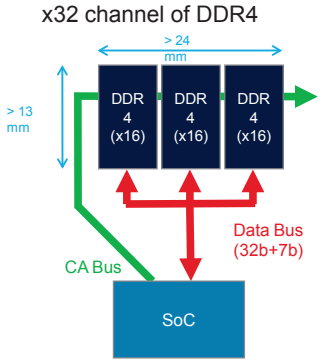
- But…
  - Cannot implement system ECC
  - In-line ECC with modern controller… performance overhead
    - Cadence controller can mitigate



DDR4 Automotive System Example

- X32 channel with ECC
- Total band width: 12.8 GBps
- Memory Capacity: 8Gb-16Gb
- Total DRAM Area: > 312 mm2

- Advantages
  - DDR4 is still the lowest cost DRAM
  - System ECC

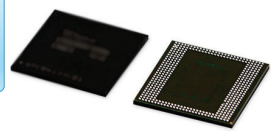


- But…
  - No X32 devices…may end up spending $ for unnecessary bits
  - Total bandwidth limited by data rates
  - Auto grade DDR4 support still evolving

LPDDR4 is Preferred Technology for Automotive

Solving memory bandwidth demand with optimized cost, power, and reliability

High Performance
- 3200-4267 data rates
- 12-17GB/s per die
- 24-34GB/s per pkg
- LPDDR4-4267 exceeds max DDR4 standard datarate



Low Power
- Low-swing I/O
- Easier frequency scaling
- Data bit inversion (DBI)
- ~40% power reduction compared to DDR4

Better Signal Integrity, Lower EM Interference
- Rich training
- Data bit inversion (DBI)
- VSS termination

DRAM vendors have committed to long-term supply of LPDDR4 for automotive production and spares

Higher Reliability
- First with post-package repair
- Extended operating range
- Temperature compensation
- DRAM vendor techniques to allow higher temp operation

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IP Design for Automotive Applications

Understand Customer Needs:

Significantly increased safety requirements on IPs

- Complexity of devices in ADAS are increasing
- Customer liability is increasing due to fully autonomous vehicle
- Safety needs to be considered early in IP development

Provide baseline safety readiness:

Safety mechanism eases meeting ASIL-ready and AECQ-100 requirements

- IP enhanced to meet fault metric target per ASIL level
- Design to grade (extended temperature range for Grade2 and Grade1)
- AECQ-100-based post-silicon characterization

Enhance system safety:

IP active safety mechanism ensures effective SoC-level safety

- Failures can be detected with high coverage and low latency
- Easy to implement localized diagnostics and recovery
- Sensible active safety features in IP reduce SoC-level safety design effort

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AEC-Q100

Characterization for hard IP example

Test Item	AEC-Q100 Requirements	Cadence Tests (Methods) Conducted
E.HBM	AEC-Q100-002E defines ESD-HBM testing to be based on ANSI/ESDA/JEDEC JS-001 Classification 2 or better Conducted at 500V, 1000V and 2000V	ESD HBM testing conducted according to ANSI/ESDA/JEDEC JS-001-2012 for 4 parts at 2000V Conclusion: • Test procedure meets AEC-Q100 requirements
E.CDM	AEC-Q100-011C1 defines ESD-CDM testing to be based on ANSI/ESD S5.3.1-2009, Charged Device Model (CDM), Component Level Classification C4B or better 750V corner pins, 500V for all other pins Sample size = (# of 250V voltage steps) x 3	ESD HBM testing conducted according to EIA/JESD22-C101_E for 4 parts at +/- 600V, +/-650V and +/-750V Conclusion: • Comparable testing procedures
E.LU	AEC-Q004D defines latch-up testing procedure compatible to JEDEC JESD78 standard Sample size: 6 parts from 1 lot	Latch-up testing conducted according to JESD78 for negative/positive current and over voltage testing on 6 parts Conclusion: • Test procedure meets AEC-Q100 requirements
E.CHAR	AEC-Q003A provides general guideline on CHAR process, CHAR plan should cover PPM target, corner lots, same sizes, etc. No hard-specific requirements provided. Sample size driven by test accuracy	CHAR plan/report: • 5 process corners: TT, FF, SS, SF, FS • Devices per corner: 5 • Junction temperature: (-40°C, 25°C, 125°C) • Supply: (LV, TV, HV) Conclusion: • 125°C junction is sufficient for Grade 2
E.TEST	Pre- and post- stress functional/parameters All samples TEST before and after HTOL at room, cold and hot temperatures	Conclusion: • Test conducted pre- and post- HTOL/ELFR stress

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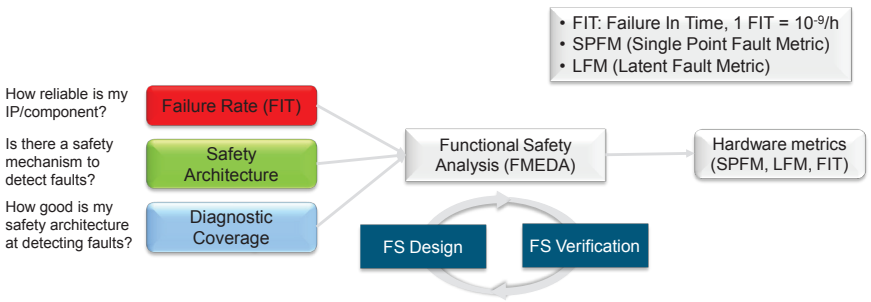
Functional Safety Analysis and Verification

Understanding and achieving ASIL hardware metrics



Functional Safety analysis
- Structured approach to measure the hardware metrics
- Drives the design/verification steps to achieve such metrics

ASIL	Failure Rate	SPFM	LFM
A	< 1000 FIT	Not relevant	Not Relevant
B	< 100 FIT	≥ 90%	≥ 60%
C	< 100 FIT	≥ 97%	≥ 80%
D	< 10 FIT	≥ 99%	≥ 90%

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Design to Grade – Implications

- Design to grade requirements
  - Grade 2 temp range -40C to 125C junction
  - Grade 1 temp range -40C to 150C junction
  - Ageing tolerance 10 or 15 year
  - ESD current tolerances
- Design challenges
  - Adopt new design rules
  - Extensive ageing simulations and signoff
  - Automotive hardened standard cells
  - Larger area to support extended temp ranges and EM rules
- PHY IP needs automotive-grade signoff and methodologies

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Automotive Safety Mechanisms

A summary of effective hardware safety mechanisms

Memory Protection
- ECC for RAM
  - 1-bit correction
  - 2-bit detection
- Parity for RAM/flash
- Checksum for ROM

State Protection
- Parity for CSRs
- Redundancy for CSRs
- Redundancy for FSM state encoding
- Illegal

Datapath Protection
- Data bus ECC
- Data bus parity
- Address bus parity
- FIFO overflow underflow
- Anti-lockup watchdog

Communication Protection
- PHY-layer BER checking
- Error correction coding
- Link-layer CRC/FCS
- Transaction-layer CRC
- Header CRC/checksum
- Illegal format detection

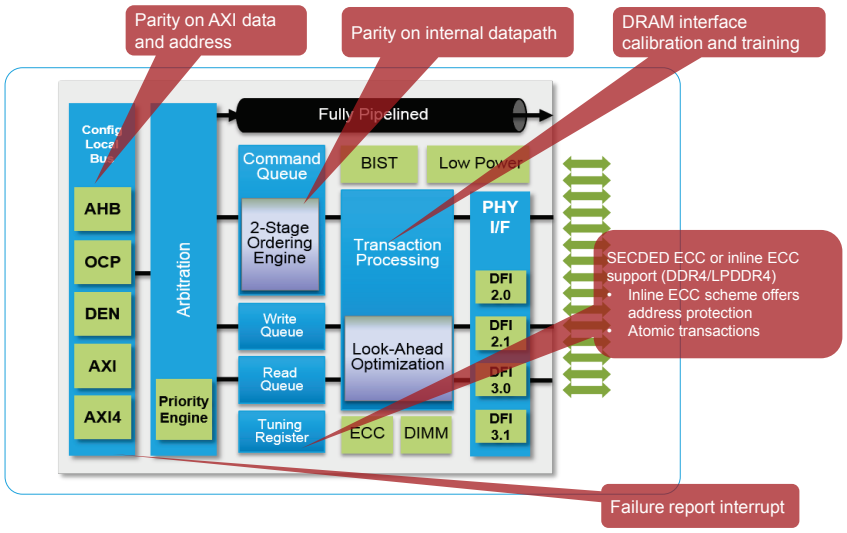
BIST
- Memory BIST
- Logic BIST
- PRBS and loopback
- Known answer test

Electrical Reliability
- Analog operating point calibration
- BER calibration
- Timing calibration and training
- Voltage, temperature monitor

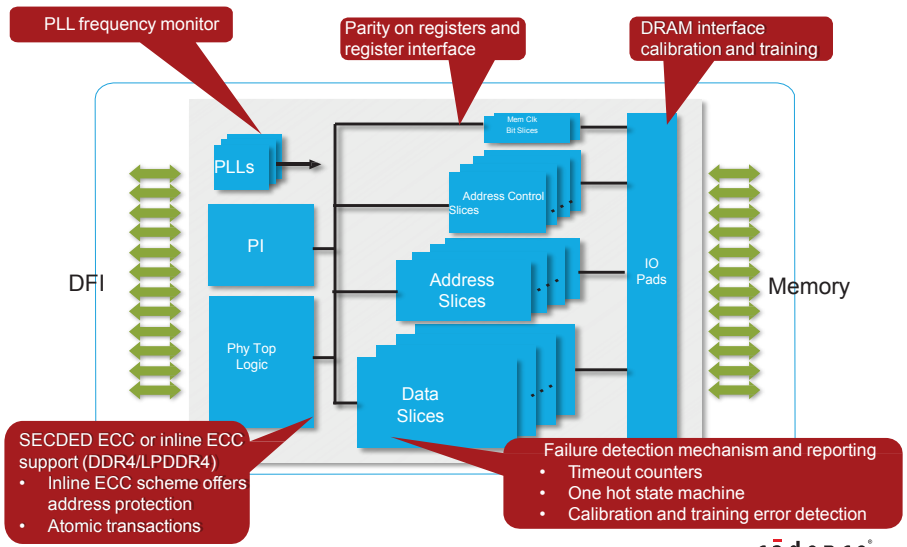
Failure Notification
- Failure notification pin
- Failure notification interrupt
- Failure status CSR and event logging counters

Failure Recovery
- Software/hardware reset
- Software/hardware initiated recalibration
- Self-correction through error correction code

Active Safety Features in DDR Controller IP



Active Safety Features in DDR PHY



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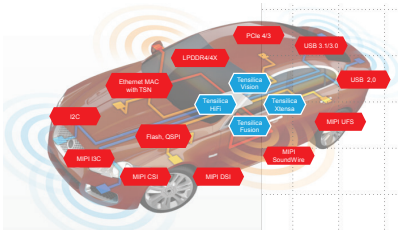
Comprehensive Automotive IP Portfolio

- Major focus and investment in automotive IP
- Commitment to functional safety
- Trained over 100 R&D engineers in ISO26262,
  - >25 achieved SGS-Tuv certifications in 2016



Hard IP	Soft IP
LPDDR4/4X PHY	LPDDR4/4X controller
PCIe4 PHY (Sierra)	PCIe4 (x16) Controller
PCIe3 PHY (Torrent)	
DP/eDP PHY (Torrent)	DP/eDP Controller
USB3.1 PHY (Torrent)	USB3.1 (10G) Controller
USB2.0 PHY	
MIPI DPHY Tx	MIPI CSI-2 Rx V1.3 Controller
MIPI DPHY Rx	MIPI CSI-2 Tx V1.3 Controller
	MIPI DSI Tx v1.3 Controller
	UFS2.1 Host controller
	QSPI
	I3C Master Controller
	Ethernet MAC with TSN

Conclusions

- Electronics demands are expanding from infotainment to ADAS to fully autonomous to improve vehicle safety
- Safety-critical applications in automotive are adopting fastest available DRAM memories as capacity and bandwidth needs increase
- LPDDR4 has become the DRAM of choice for automotive electronics due to its superior bandwidth for a given memory size
- LPDDR4 memory controller and PHY interface designs must consider functional safety, long-term reliability, and temperature range requirements
- Cadence DDR IP solutions are automotive ready and available now

